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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,193	11/21/2003	Thaddeus John Gabara	91-2-36	2999

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,193	GABARA ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *April 13, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 17-20* is/are rejected.

7)☐ Claim(s) *13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Base on the Pre-Appeal Brief Conference with SPEs Tom Thomas and Robert Pascal and Examiner Hollington, all parties agree to withdraw the finality of the previous Office Action mailed on January 9, 2006. Below is a new Office Action provided by Examiner Hollington.

The indicated allowability of claims 2, 5 and 9 is withdrawn in view of the newly discovered reference(s) to admitted prior art of Fig. 2 in view of Farnworth et al. Rejections based on the newly cited reference(s) follow

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art of Fig. 2 in view of Farnworth et al (5059899).

Regarding claims 1and 19, Admitted prior art of Fig. 2 discloses an apparatus (IC chip) comprising an integrated circuit die (IC die 100') comprising a internal signal pad (part of array of pads 106) arranged at a location away from a periphery of the die (100'), a peripheral signal pad (buffer circuit pad 102) arranged proximate the periphery of the die (100'). However, the admitted prior art does not include a switch as claimed. Farnworth et al disclose an apparatus (wafer 10) comprising an integrated circuit die (IC die 30) comprising a internal signal pad (bonding pad 34) arranged at a location away from a periphery of the die (30), a peripheral signal pad (test pad 36) arranged proximate the periphery of the die (30) and a switch (transistor switch 40) coupled between the internal signal pad (34) and the peripheral signal pad (36) [via test circuitry 46]; the switch (40) being configurable in at least a first state in which the internal signal pad is not operatively connected to the peripheral signal pad (36), and a second state in which the internal signal pad (34) is operatively connected to the peripheral signal pad (36); the switch (40) being configurable in one of the first and second states responsive to a control signal [via test circuitry 46] having one of first and second signal characteristics, respectively; wherein the switch (40) is configured in the first state during normal operation of the integrated circuit die (30); and wherein the switch (40) is configured in the second state to permit test access to the internal signal pad (34) via the peripheral signal pad (36). Further, Farnworth et al teach that the addition of the switch (40) is advantageous because it connects the pad inside the die to the test pad for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the admitted prior art of Fig. 2 by adding a switch between an internal pad and peripheral pad as taught by Farnworth et al in order to connect the

two pads for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer to determine if the die is good or not good to use.

Regarding claim 2, Admitted prior art of Fig. 2 discloses at least one of the internal signal pad (part of 106) and the peripheral signal pad (102) comprises a bonding pad (104).

Regarding claim 3, Admitted prior art of Fig. 2 discloses at least one of the internal signal pads (part of 106) and the peripheral signal pad (102) has a buffer circuit (102) associated therewith.

Regarding claim 4, Admitted prior art of Fig. 2 discloses the internal signal pad (part of 106) is part of an area array (array 106) of the integrated circuit die (100').

Regarding claim 5, Admitted prior art of Fig. 2 discloses the internal signal pad (part of 106) comprises an analog signal pad (not numbered but shown).

Regarding claim 6, Admitted prior art of Fig. 2 discloses the internal signal pad (part of 106) and the peripheral signal pad (102). However, it does not disclose the switch as claimed. Farnworth et al disclose an apparatus (wafer 10) comprising an integrated circuit die (IC die 30) comprising a internal signal pad (bonding pad 34) arranged at a location away from a periphery of the die (30), a peripheral signal pad (test pad 36) arranged proximate the periphery of the die (30) and a switch (transistor switch 40), wherein the switch (40) is arranged nearer to the internal signal pad (34) than to the peripheral signal pad (36). Further, Farnworth et al teach that the addition of the switch (40) is advantageous because it connects the pad inside the die to the test pad for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the admitted prior art of Fig. 2 by adding a switch

between an internal pad and peripheral pad as taught by Farnworth et al in order to connect the two pads for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer to determine if the die is good or not good to use.

Regarding claim 7, Admitted prior art of Fig. 2 discloses the internal signal pad (part of 106) and the peripheral signal pad (102). However, it does not disclose the switch as claimed. Farnworth et al disclose an apparatus (wafer 10) comprising an integrated circuit die (IC die 30) comprising a internal signal pad (bonding pad 34) arranged at a location away from a periphery of the die (30), a peripheral signal pad (test pad 36) arranged proximate the periphery of the die (30) and a switch (transistor switch 40), wherein the switch (40) is arranged immediately adjacent to the internal signal pad (34), so as to minimize parasitic elements associated with the signal pad (34) when the switch (40) is in the first state. Further, Farnworth et al teach that the addition of the switch (40) is advantageous because it connects the pad inside the die to the test pad for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the admitted prior art of Fig. 2 by adding a switch between an internal pad and peripheral pad as taught by Farnworth et al in order to connect the two pads for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer to determine if the die is good or not good to use.

Regarding claim 8, Farnworth et al disclose the test access to the signal pad (34) via the peripheral signal pad (36) involves establishing electrical contact between inherently an external probe [not shown but see col. 2, line 65- col. 3, line 16] and the peripheral signal pad (36).

Regarding claim 9, Farnworth et al disclose the inherently external probe comprises a test probe of a wire-type wafer probe card.

Regarding claim 10, Admitted prior art of Fig. 2 discloses the internal signal pad (part of 106) and the peripheral signal pad (102). However, it does not disclose the switch as claimed. Farnworth et al disclose an apparatus (wafer 10) comprising an integrated circuit die (IC die 30) comprising a internal signal pad (bonding pad 34) arranged at a location away from a periphery of the die (30), a peripheral signal pad (test pad 36) arranged proximate the periphery of the die (30) and a switch (transistor switch 40), wherein the switch (40) is configured in the second state in conjunction with wafer-level testing of the integrated circuit die (30) prior to separation of the die (30) from a corresponding semiconductor wafer (10). Further, Farnworth et al teach that the addition of the switch (40) is advantageous because it connects the pad inside the die to the test pad for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the admitted prior art of Fig. 2 by adding a switch between an internal pad and peripheral pad as taught by Farnworth et al in order to connect the two pads for the purpose of enabling electrical access to the pad inside the die for testing the die before dicing the wafer to determine if the die is good or not good to use.

Regarding claim 11, Admitted prior art of Fig. 2 discloses the integrated circuit die (100). However, it does not disclose a control circuit as claimed. Farnworth et al disclose an apparatus (wafer 10) comprising an integrated circuit die (IC die 30) comprising a internal signal pad (bonding pad 34) arranged at a location away from a periphery of the die (30), a peripheral signal pad (test pad 36) arranged proximate the periphery of the die (30) and a switch (transistor switch

40), wherein the integrated circuit die (30) comprises a control circuit (control line 42) configured to generate the control signal for controlling the state of the switch (40). Further, Farnworth et al teach that the addition of the control circuit (42) is advantageous because it enables electrical access to the pad within individual dies for the purpose controlling the on and off function of the switch so to avoid the possibility of a short or inducing voltages going into the die. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the admitted prior art of Fig. 2 by adding a control circuit in the die as taught by Farnworth et al in order to electrical access to the pad within individual dies for the purpose controlling the on and off function of the switch to avoid damaging the die under test.

Regarding claim 12, Farnworth et al disclose the control signal (42) having one of the first and second signal characteristics comprises the control signal (42) being at one of a first signal level and a second signal level, respectively.

Regarding claim 18, the admitted prior art discloses the integrated circuit die (100') is inherently part of a semiconductor wafer (not shown) containing a plurality of dies (not shown).

3. Claims 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art of Fig. 2 in view of Farnworth et al above, and further in view of Fredrickson (6681352).

Regarding claim 17, the admitted prior art in view of Farnworth et al disclose an apparatus comprising an integrated circuit die (100') comprising a signal pad (part of array probes 106) arranged at a location away from a periphery of the die, a peripheral signal pad (102) arranged proximate the periphery of the die, and a switch (switch 40 in Farnworth et al) coupled

between the signal pad (34 of Farnworth) and the peripheral signal pad (36 of Farnworth). However he does not disclose the integrated circuit die is packaged as claimed. Fredrickson discloses [see Fig. 2a] the integrated circuit die (semiconductor die 110) is packaged within packaged integrated circuit (IC package 200). Further, Fredrickson teach that the addition of die in the IC package is advantageous because it provides that the die is a functional die and the package is used to by customers for varies testing function. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Whetsel by adding the die into a package as taught by Fredrickson in order to provide a functional die to be sent to customers for varies testing purposes.

Regarding claim 20, admitted prior art of Fig. 2 in view of Farnworth et al discloses an apparatus comprising an integrated circuit die (100') comprising a signal pad (part of array of pads 106) arranged at a location away from a periphery of the die, a peripheral signal pad (102) arranged proximate the periphery of the die (100'), and a switch (switch 40 of Farnworth) coupled between the signal pad (34 of Farnworth) and the peripheral signal pad (36 of Farnworth); the switch (40) being configurable in at least a first state in which the signal pad (34) is not operatively connected to the peripheral signal pad (36), and a second state in which the signal pad (34) is operatively connected to the peripheral signal pad (36); the switch (40) being configurable in one of the first and second states responsive to a control signal having one of first and second signal characteristics, respectively; wherein the switch (40) is configured in the first state during normal operation of the integrated circuit die (30); and wherein the switch (40) is configured in the second state to permit test access to the signal pad (34) via the peripheral signal pad (36). However, he does not disclose a package integrated circuit with a lead frame coupled to

the die as claimed. Fredrickson disclose [see Fig. 2A] a packaged integrated circuit (IC package 200) comprising an integrated circuit die (semiconductor die 110); a lead frame (metal leads 220) coupled to the die (110); the integrated circuit die (110) and lead frame (220) being at least partially enclosed by a packaging material (package body 210). Further, Fredrickson teach that the addition of die in the IC package is advantageous because it provides that the die is a functional die and the package is used to by customers for varies testing function. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Whetsel by adding the die into a package as taught by Fredrickson in order to provide a functional die to be sent to customers for varies testing purposes.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Parrish (5053700) discloses a method for wafer scale testing of redundant IC dies.

Allowable Subject Matter

5. Claims 13-16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: regarding claim 13, the primary reason for the allowance of the claim is due to an apparatus comprising a control circuit comprises at least one inverter, an output of the inverter being

coupled to a control signal input of the switch. Since claims 14-16 depend from claim 13, they also have allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
May 3, 2006